Abstracts

10 Gb/s clock extraction and data regeneration circuit implemented with phase-locked loop

Tae-Whan Yoo and Moon-Soo Park. "10 Gb/s clock extraction and data regeneration circuit implemented with phase-locked loop." 1997 MTT-S International Microwave Symposium Digest 3. (1997 Vol. III [MWSYM]): 1713-1716.

A PLL clock-extraction and data-regeneration circuit (CEDAR) for 10 Gb/s optical transmission system was realized in a hybrid IC form. The jitter characteristics satisfied the recommendations of ITU-T. The CEDAR compensated against the temperature was tested for the temperature from -10/spl deg/C to 60/spl deg/C and showed no increase of error.

❑ Return to main document.